What I claim is:

1. A semiconductor device with an array of flash memory cells comprising:

a semiconductor substrate;

a repeated cell arranged in columns and rows and comprising transistors with floating gates;

in each cell a common source for adjacent transistors;

first and second floating gates on opposite sides of the common source;

first and second drains, respectively, on the other side of the first and second floating gates;

wherein the common sources are connected together in a buried bit line in the substrate and the drains are aligned with each other and connected to a metal contact layer disposed over the substrate and aligned with the drains and source.

2. The device of claim 1 further comprising a deep trench disposed between adjacent columns for isolating the transistors in each column from the transistors in the adjacent columns.

3. The device of claim 2 having a substrate of a first polarity, a deep well of a second and opposite polarity, wherein the deep trench extends to or beyond the depth of the deep well of the second polarity.

4. The device of claim 1 wherein each common source has a body tie of opposite polarity to the source polarity.

5. The device of claim 4 wherein the body ties are self-aligned to spacers on the gates of the transistors.

6. The device of claim 2 wherein the deep trench isolation regions provide capacitors for charge pumps for the memory cells.

7. The device of claim 1 further comprising logic or linear devices disposed on the surface and separated from each other by shallow trench isolation regions.

8. A semiconductor device with a flash memory array comprising a plurality of floating gate transistors, said transistors arranged with their sources and drains aligned in columns;

a plurality of word lines extending transverse to the column to form a plurality of rows, with each word line connected to the floating gates of the transistors beneath the word line;

each column comprising a plurality of first and second floating gate transistors wherein each first and second floating gate transistor has a drain, a source and floating gate between its drain and source;

a common source region disposed between opposite sides of the first and second floating gates and providing the sources for two adjacent transistors;

a deep trench disposed between adjacent columns for isolating the transistors in each column from the transistors in the adjacent columns;

a first and second drain regions disposed respectively on the other sides of the first and second floating gates;

a plurality of first bit line buried beneath the surface of the substrate and connecting together in each column the common sources of the floating gate transistors;

drain contacts aligned with each other in the same columns as the sources for contacting the first and second drains of the first and second floating gate transistors in each column;

an insulation layer over the substrate for laterally isolating drain contacts from each other;

a plurality of second bit lines, each second bit line extending substantially parallel to its corresponding column, over the insulation layer and extending through the insulation layer to contact the drain contacts in each column of the array.

9. The semiconductor device of claim 8 having a substrate of a first polarity, a deep well of a second and opposite polarity, wherein the deep trench extends to or beyond the depth of the deep well of the second polarity.

10. The semiconductor device of claim 8 wherein each common source has a body tie of opposite polarity to the source polarity.

11. The semiconductor device of claim 10 wherein the body ties are self-aligned to spacers on the gates of the transistors.

12. The semiconductor device of claim 8 wherein the deep trench isolation regions provide capacitors for charge pumps for the memory cells.

13. The semiconductor device of claim 8 further comprising logic or linear devices disposed on the surface and separated from each other by shallow trench isolation regions.

14. A semiconductor device having a memory array comprising:

memory cells in a semiconductor substrate;

a word line that includes control electrodes for a first plurality of the memory cells,

a first bit line electrically connecting first current carrying electrodes for a second plurality of the memory cells; and

a second bit line electrically connecting second current carrying electrodes of a third plurality of the memory cells; and

wherein within the memory array, a first bit buried in the substrate, and second bit line disposed over the substrate, vertically spaced from the first bit line, and extending substantially parallel to the first bit line and at an elevation different from the word line.

15. The semiconductor device of claim 14 further comprising a deep trench disposed between adjacent columns for isolating the transistors in each column from the transistors in the adjacent columns.

16. The semiconductor device of claim 14 having a substrate of a first polarity, a deep well of a second and opposite polarity, wherein the deep trench extends to or beyond the depth of the deep well of the second polarity.

17. The semiconductor device of claim 14 wherein each common source has a body tie of opposite polarity to the source polarity.

18. The semiconductor device of claim 17 wherein the body ties are self-aligned to spacers on the gates of the transistors.

19. The semiconductor device of claim 15 wherein the deep trench isolation regions provide capacitors for charge pumps for the memory cells.

20. The semiconductor device of claim 14 further comprising logic or linear devices disposed on the surface and separated from each other by shallow trench isolation regions.

21. A system on chip semiconductor device comprising:

a plurality of logic devices;

a plurality of linear devices;

shallow trench isolation regions separating the logic devices from each other and separating the linear devices from each other;

an array of memory cells comprising:

a word line that includes control electrodes for a first plurality of the memory cells,

a first bit line electrically connecting first current carrying electrodes for a second plurality of the memory cells; and

a plurality of columns, each column having

a second bit line electrically connecting second current carrying electrodes of a third plurality of the memory cells;

a deep trench disposed between adjacent columns for isolating the transistors in each column from the transistors in the adjacent columns; and

wherein within the memory cell array, a first bit buried in the substrate, and second bit line disposed over the substrate, vertically spaced from the first bit line, and extending substantially parallel to the first bit line and at an elevation different from the word line.

22. The semiconductor device of claim 21 having a substrate of a first polarity, a deep well of a second and opposite polarity, wherein the deep trench extends to or beyond the depth of the deep well of the second polarity.

23. The semiconductor device of claim 21 wherein each common source has a body tie of opposite polarity to the source polarity.

24. The semiconductor device of claim 21 wherein the body ties are self-aligned to spacers on the gates of the transistors.

25. The semiconductor device of claim 21 wherein the deep trench isolation regions provide capacitors for charge pumps for the memory cells.

26. A process for fabricating a system on chip device in a semiconductor substrate, the device having low power logic devices, higher power driver devices and a flash memory array comprising a plurality of floating gate transistors, said floating gate transistors arranged with their sources and drains aligned in columns;

forming a plurality of word lines extending transverse to the columns to form a plurality of rows, with each word line connected to the floating gates of the transistors beneath the word line;

forming columns comprising a plurality of first and second floating gate transistors wherein each first and second floating gate transistor has a drain, a source and floating gate between its drain and source;

in each column forming common source regions disposed between opposite sides of the first and second floating gates to provide the sources for two adjacent transistors;

in each column forming first and second drain regions disposed respectively on the other sides of the first and second floating gates;

in each column forming drain contacts aligned with the sources for contacting the first and second drains of the first and second floating gate transistors in each column;

in each column forming a first bit lines buried beneath the surface of the substrate for connecting together the common sources of the floating gate transistors;

in each column forming a second raised bit line disposed over the substrate and over the buried bit line and having contacts extending to the surface to contact the drains on floating gate transistors in the column; and

forming a deep trench disposed between adjacent columns for isolating the transistors in each column from the transistors in the adjacent columns.

27. The process of claim 26 further comprising implanting body tie dopants into the source regions to form body ties and siliciding the body ties.

28. The process of claim 26 wherein the body tie implants have a polarity opposite to the polarity of the source regions.

29. The process of claim 26 comprising:

forming first wells of a polarity opposite the polarity of the sources and drains;

forming seconds wells surrounding the first wells and of a polarity the same as the sources and drains;

forming third wells of a polarity the same as the first well;

forming the deep trenches deep enough to penetrate the second wells.

30. The process of claim 26 wherein the third wells comprises the substrate.